CLAIMS

I claim:

1. An apparatus, comprising:

a semiconductor chip;

a first contact site on the semiconductor chip;

a dominant driving circuit having a first input and a first output coupled to the first contact site, the first output having a variable drive strength responsive to the first input;

a subordinate driving circuit having a second input and a second output coupled to the first contact site, the second output having a variable drive strength responsive to the second input;

a test control circuit having a test mode, at least one output coupled to the first input of the first driving circuit, and at least one output coupled to the second input of the second driving circuit,

the test control circuit operable in test mode to create a drive fight between the dominant and subordinate driving circuits, and to generate a test value at the first contact site;

a second contact site on the semiconductor chip for probing; and

a gated signal path connecting the second contact site to the first contact site, operable in test mode to transfer the test value from the first contact site to the second contact site.

2. An apparatus as in claim 1, wherein the test control circuit is operable in the test mode to select a greater output drive strength for the dominant driving circuit than for the subordinate driving circuit, and generate a test value at the first contact site that is indicative of the functionality of the dominant driving circuit.

3. An apparatus as in claim 2, wherein the dominant driving circuit includes

a first parallel circuit having a plurality of branches connected in parallel between the first contact site and a first node, at least one branch of the first parallel circuit including at least one transistor.

4. An apparatus as in claim 3, wherein each branch of the first parallel circuit includes a transistor.

5. An apparatus as in claim 4, wherein the test control circuit is operable in the test mode to enable a number of transistors required in the dominant driving circuit to overdrive the subordinate driving circuit.

6. An apparatus as in claim 5, wherein the signal path includes

a shift register for capturing the test value from the first contact site and shifting it to the second contact site.

7. An apparatus as in claim 6, wherein the shift register includes at least one boundary scan cell.

8. An apparatus as in claim 5, wherein the first node is for connection to a power source.

9. An apparatus as in claim 5, wherein the first node is for connection to a ground.

10. An apparatus as in claim 5, wherein the subordinate driving circuit includes

a second parallel circuit having a plurality of branches connected in parallel between the first contact site and a second node, at least one branch of the second parallel circuit including at least one transistor.

11. An apparatus as in claim 10, wherein each branch of the second parallel circuit includes a transistor.

12. An apparatus as in claim 2, wherein the test control circuit includes a plurality of scan flip-flops linked together to form a scan shift register, at least one scan flip-flop having an output coupled to an input of the dominant driving circuit.

13. A method for testing an input/output (I/O) pad on a semiconductor chip, comprising:

selecting a first drive strength for a first driving circuit;

selecting a second drive strength for a second driving circuit, the first drive strength greater than the second drive strength;

driving a first contact site of the I/O pad with both the first and second driving circuits;

generating a test value at the first contact site indicative of the drive strength of the first driving circuit; and

transferring the test value to a second contact site on a second I/O pad.

14. A method as in claim 13, further comprising:

probing the second contact site with an external prober to determine the test value.

15. A method as in claim 13, wherein transferring the test value includes:

shifting the test value through a boundary shift register.

16. A method as in claim 14, wherein selecting a first drive strength includes:

enabling a branch in a parallel circuit in the first driving circuit.

17. A method as in claim 15, wherein selecting a second drive strength includes:

enabling a branch in a parallel circuit in the second driving circuit.